

Huawei Atlas 200

Technical White Paper

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About This Document

Purpose

This document describes the Atlas 200 AI accelerator module (Atlas 200 for short) in detail, including its appearance, performance parameters, and configuration application.





Intended Audience


This document is intended for:

- Huawei presales engineers
- Channel partner presales engineers
- Enterprise presales engineers

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
	Indicates an imminently hazardous situation which, if not avoided, will result in death or serious injury.
	Indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury.
	Indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury.
	Indicates a potentially hazardous situation which, if not avoided, could result in equipment damage, data loss, performance deterioration, or unanticipated results. NOTICE is used to address practices not related to personal injury.

Symbol	Description
 NOTE	<p>Calls attention to important information, best practices, and tips.</p> <p>NOTE is used to address information not related to personal injury, equipment damage, and environment deterioration.</p>

Change History

Issue	Date	Description
02	2019-07-27	This issue is the second official release.
01	2019-05-21	This issue is the first official release.

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1 Product Introduction

[1.1 Overview](#)

[1.2 Appearance](#)

[1.3 System Architecture](#)

1.1 Overview

The Atlas 200 AI accelerator module is a high-performance AI compute module.

By integrating the HiSilicon Ascend 310 AI processor, the Atlas 200 is ideal for analysis and inferential computing of data such as images and videos. It can be widely used in intelligent surveillance, robots, drones, and video servers.

NOTE

Ascend 310 is a high-performance and low-power artificial intelligence (AI) chip designed for image recognition, video processing, inference computing, and machine learning. The chip has two built-in AI core chips that support the 128-bit LPDDR4X and a maximum computing capability of 16 TOPS (INT8).

1.2 Appearance

The Atlas 200 uses a compact structure of 38.5 mm x 52.6 mm. Two heights, 4.3 mm and 6 mm are available for you to select based on your connector type, supporting flexible installation.

The Atlas 200 complies with section 15 of the Federal Communications Commission (FCC) rule. Operation is subject to the following two conditions:

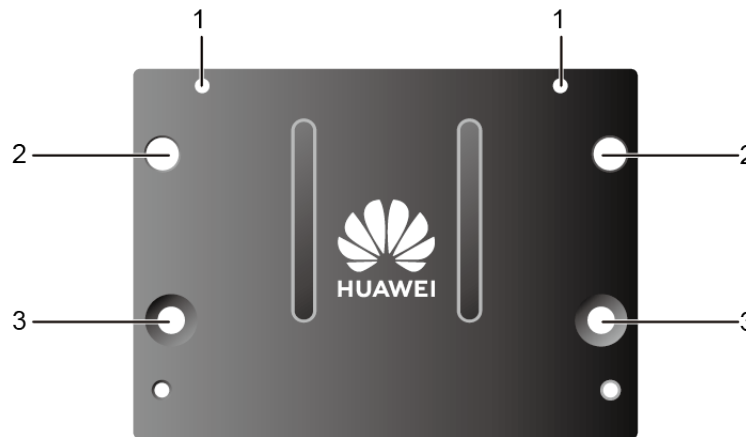
- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation.

Figure 1-1 shows the appearance of the Atlas 200.

Figure 1-1 Appearance of the Atlas 200

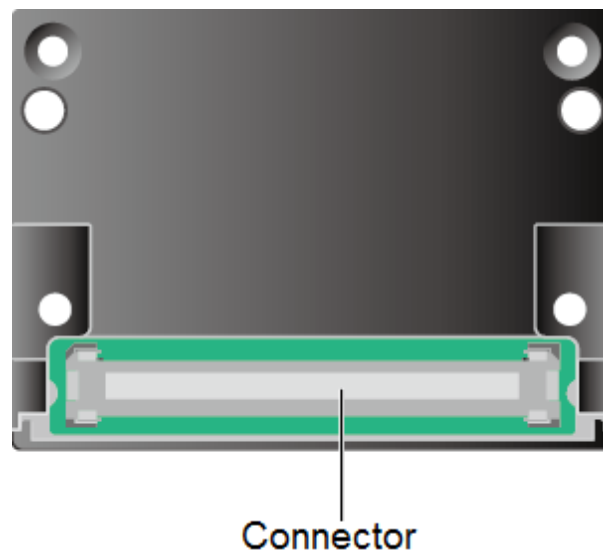


Figure 1-2 Atlas 200 front panel



1	Guide hole	2	Mounting hole
3	Heat sink hole	-	-

Figure 1-3 Rear panel and connector

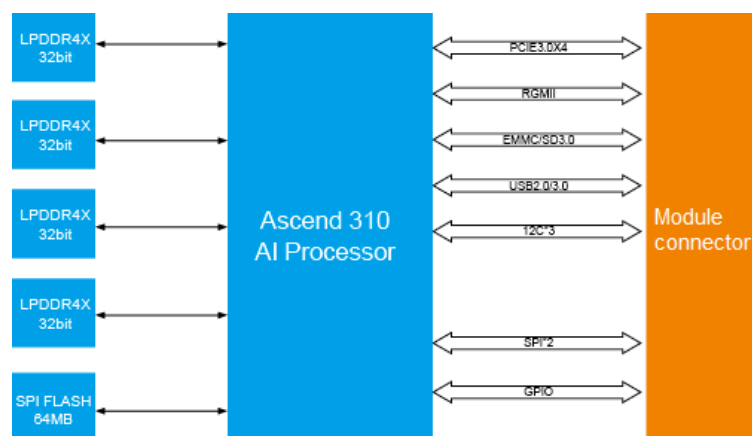


1.3 System Architecture

The Atlas 200 integrates a complete Ascend 310 AI processor hardware system, which shortens the R&D period and simplifies the user design.

Figure 1-4 shows the system architecture of the Atlas 200.

Figure 1-4 System architecture of the Atlas 200



2 Product Features

2.1 Performance

2.2 Maintainability

2.1 Performance

- Powered by high-performance Huawei Ascend 310 AI processor, the Atlas 200 provides the 16 TOPS INT8 or 8 TOPS FP16 multiply-add computing capability.
- Provides various interfaces and supports PCIe 3.0 x4, RGMII, USB 2.0/USB 3.0, I²C, SPI and UART interfaces.
- Supports up to 16-channel 1080p@30 fps video access.
- Supports H.264 and H.265 video encoding and decoding in various specifications, which can be applicable to different video processing requirements.

2.2 Maintainability

- Supports in-band online upgrades to facilitate routine maintenance.
- Obtains device information such as the temperature and voltage status in-band and out-of-band and simplifies management through the graphical user interface (GUI).
- Provides comprehensive command line management functions for users to perform routine device management by using various commands.
- Provides information such as the production dates and serial numbers to facilitate in-band and out-of-band asset management.

3 Product Specifications

3.1 Basic Specifications

3.2 Environmental Conditions

3.1 Basic Specifications

Table 3-1 Hardware specifications of the Atlas 200

Feature	Specification
AI processor	<ul style="list-style-type: none">● Two DaVinci AI cores● CPU: 8-core A55, max 1.6 GHz
AI computing capability	<ul style="list-style-type: none">● Multiply-add computing performance: 8 TFLOPS/FP16, 16 TOPS/INT8
Memory	<ul style="list-style-type: none">● 128-bit LPDDR4X● Capacity: 8 GB/4 GB● Interface rate: 3200 Mbit/s
Error checking and correction (ECC)	Supports ECC.
Storage device	<ul style="list-style-type: none">● Built-in SPI flash. Capacity: 64 MB● External MMC interfaces and supports:<ul style="list-style-type: none">- eMMC 4.5 granular, supporting the highest mode SDR50 and a maximum capacity of 64 GB- SD3.0 card, supporting the highest mode SDR50 and a maximum capacity of 2 TB

Feature	Specification
Encoding and decoding capability	<ul style="list-style-type: none"> ● H.264 hardware decoding at 16-channel 1080p@30 fps (2-channel 3840 x 2160@60 fps) in the YUV420 format ● H.265 hardware decoding at 16-channel 1080p@30 fps (2-channel 3840 x 2160@60 fps) in the YUV420 format ● H.264 hardware encoding at 1-channel 1080p@30 fps in the YUV420 format ● H.265 hardware encoding at 1-channel 1080p@30 fps in the YUV420 format ● JPEG decoding capability at 1080p 256 fps and encoding capability at 1080p 64 fps, and a maximum resolution of 8192 x 8192 ● PNG decoding capability at 1080p 48 fps, and a maximum resolution of 4096 x 4096
High-speed interface	<ul style="list-style-type: none"> ● PCIe 3.0 x4 lane, supports RC or EP mode ● RGMII: 1 port ● USB2.0/USB3.0: 1 lane
Serial bus	<ul style="list-style-type: none"> ● UART: 2 ports ● I²C: 3 ports ● SPI: 3 ports (multiplexed with SPI3, I²C2, and UART1 signals)
Other interfaces	<ul style="list-style-type: none"> ● eMMC & SD: 1 port ● Atlas 200 power-on signal x1 ● Atlas 200 reset signal x1 ● PWM x2 ● GPIO x4
Interface specifications	<ul style="list-style-type: none"> ● 144-pin board to board (BTB) connector ● Height requirements of 4.3 mm (0.17 in.) and 6 mm (0.24 in.)
Power consumption	<ul style="list-style-type: none"> ● Operating voltage: 3.5 V to 4.5 V. Recommended typical value: 3.8 V. ● Typical power consumption: 11 W
Structure and dimensions	52.6 mm x 38.5 mm x 8.5 mm (2.07 in. x 1.52 in. x 0.33 in.) NOTE The model of the Atlas 200 connector is fixed. Users can choose male sockets with different heights to configure the height of different Atlas 200s.
Weight	30 g

Table 3-2 Basic specifications of the Atlas 200 software

Feature	Specification
Operating system (OS)	Ubuntu 16.04
Deep learning framework	TensorFlow, Caffe
Compiler	CCE/CCE compiler Tool

3.2 Environmental Conditions

The Atlas 200 is applicable to various working scenarios, such as video surveillance devices, UAVs, and servers. The Atlas 200 adopts a high-specification hardware design to meet demanding environment requirements.

Table 3-3 Environment requirements of the Atlas 200

Item	Specification
Operating temperature	-25°C to +80°C (-13°F to +176°F)
Storage temperature	-25°C to +85°C (-13°F to +185°F)
Relative humidity (RH, non-condensing)	5% to 90%
Storage humidity (RH, non-condensing)	5% to 95%
Maximum altitude	5000 m (16404.20 ft.) For altitudes from 1800 m (5905.51 ft.) to 5000 m (16404.20 ft.), the highest operating temperature decreases by 1°C (1.8°F) for every increase of 220 m (721.78 ft.) in altitude.

4 Certifications

Table 4-1 Certifications.

No.	Country/Region	Certification	Standard
1	Europe	CE	Safety: <ul style="list-style-type: none"> ● IEC 60950-1:2005(2nd Edition)+A1:2009+A2:2013 ● EN 60950-1:2006+A11:2009+A1:2010+A12:2011+A2:2013 EMC: <ul style="list-style-type: none"> ● EN 55032:2012/AC:2013 ● CISPR 32:2012 ● EN 55032:2015 ● CISPR 32:2015 ● EN 55024:2010 ● CISPR 24:2010 ● EN 55024:2010+A1:2015 ● CISPR 24:2010+A1:2015 ● ETSI EN 300 386 V1.6.1:2012 ● ETSI EN 300 386 V2.1.1:2016 ● EN61000-3-3:2013 ● EN61000-6-2:2005

No.	Country/Region	Certification	Standard
			● EN61000-6-4:2006+ A1:2010
2	Europe	RoHS	EN 50581: 2012
3	Japan	VCCI	VCCI 32-1

5 Warranty

For details, see the [Maintenance & Warranty](#).

A Acronyms and Abbreviations

A	
AI	Artificial Intelligence
B	
BTB	Board to Board Connector
E	
ECC	Error Checking and Correction
eMMC	Embedded Multimedia Card
F	
FLOPS	Floating-point Operations Per Second
I	
I²C	Inter-integrated Circuit
L	
LPDDR	Low-power Double Data Rate
P	
PCIe	Peripheral Component Interconnect Express
PWM	Pulse-width Modulation
R	
RGMI	Reduced Gigabit Media Independent Interface
S	
SPI	Serial Peripheral Interface
T	
TFLOPS	teraFLOPS

U

USB

Universal Serial Bus

UART

Universal Asynchronous Receiver/transmitter