|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | | |  |
|  | | |
|  | | |
|  | | | |
|  | **HUAWEI S12700 Series Agile Switches** | |  |
|  | |
| **Issue** | **01** |
| **Date** | **2014-2-21** |
|  | |
| HUAWEI TECHNOLOGIES CO., LTD. | |
|  | | |

|  |
| --- |
| Copyright © Huawei Technologies Co., Ltd. 2014. All rights reserved.  No part of this document may be reproduced or transmitted in any form or by any means without prior written consent of Huawei Technologies Co., Ltd.  Trademarks and Permissions  and other Huawei trademarks are trademarks of Huawei Technologies Co., Ltd.  All other trademarks and trade names mentioned in this document are the property of their respective holders.  Notice  The purchased products, services and features are stipulated by the contract made between Huawei and the customer. All or part of the products, services and features described in this document may not be within the purchase scope or the usage scope. Unless otherwise specified in the contract, all statements, information, and recommendations in this document are provided "AS IS" without warranties, guarantees or representations of any kind, either express or implied.  The information in this document is subject to change without notice. Every effort has been made in the preparation of this document to ensure accuracy of the contents, but all statements, information, and recommendations in this document do not constitute a warranty of any kind, express or implied. |

|  |  |
| --- | --- |
| Huawei Technologies Co., Ltd. | |
| Address: | Huawei Industrial Base  Bantian, Longgang  Shenzhen 518129  People's Republic of China |
| Website: | [http://www.huawei.com](http://www.huawei.com/) |
| Email: | [support@huawei.com](mailto:Support@huawei.com) |

Contents

[1 S12700 Series Agile Switches Overview 1](#_Toc382465567)

[1.1 Introduction 1](#_Toc382465568)

[1.2 S12708 Hardware architecture 1](#_Toc382465569)

[1.3 S12712 Hardware architecture 2](#_Toc382465570)

[2 Key Technologies 1](#_Toc382465571)

[2.1 S12700 System Architecture 1](#_Toc382465572)

[2.2 MPU Hardware Design 2](#_Toc382465573)

[2.3 SFU Hardware Design 4](#_Toc382465574)

[2.1 Hardware Design of X1E Series Interface Cards 5](#_Toc382465575)

[2.2 Hardware Design of a 48\*10GE Interface Card 8](#_Toc382465576)

# S12700 Series Agile Switches Overview

## Introduction

The S12700 series agile switches are fully programmable core switches designed for next-generation campus networks. The switches use the industry's first Ethernet network processor (ENP). The chip's flexible packet processing and traffic control capabilities can meet current and future service requirements, helping build a highly scalable network. In addition to capabilities of common switches, the S12700 series provides fully programmable open interfaces and supports programmable forwarding behaviors. Enterprises can use the open interfaces to develop new protocols and functions independently or jointly with equipment vendors to build campus networks meeting their own needs.

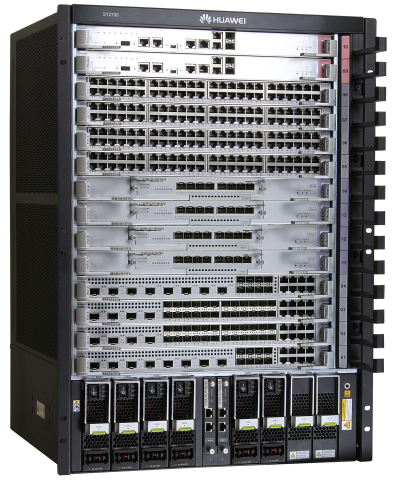
The S12700 series uses independent switch fabric units (SFUs) to provide large-capacity, highly reliable switching service. As the control and switching engines are independent of each other, control service flows are separated from data service flows. The system can still function normally when a single engine fails. An S12700 agile switch supports four SFUs, which perform parallel data switching to improve the system switching capacity. The four SFUs in an S12700 chassis works in 3+1 redundancy mode. Failure of a single SFU does not affect service forwarding. This SFU redundancy design improves system reliability.

The S12700 series has the following characteristics:

* Uses the innovative ENP, which provides flexible packet processing and flow control capabilities to support current service development and help cope with challenges in the future.
* Separates the control engines from the switching engines and supports 3+1 redundancy of SFUs, enhancing system reliability.
* Supports Cluster Switching System generation 2 (CSS2). CSS2 is the industry's first switch fabric hardware clustering technology. A cluster set up using this technology supports 1+N backup of Main Processing Units (MPUs). The cluster bandwidth is up to 640 Gbit/s, which will be expanded to 1.92 Tbit/s in the future.
* Provides hardware OAM and BFD functions using the hardware detection engine integrated on MPUs. These hardware detection technologies implement high-precision fault detection and 50 ms failover.

The S12700 series is available in two models: S12708 and S12712. An S12708 chassis supports a maximum of eight Line Processing Units (LPUs). An S12712 chassis supports a maximum of 12 LPUs. Key components of the S12708 and S12712, such as MPUs, SFUs, LPUs, Centralized Monitoring Units (CMU), power modules, and fan modules, can work in redundancy mode to ensure hardware reliability. Figure 1-1 shows the two chassis models.

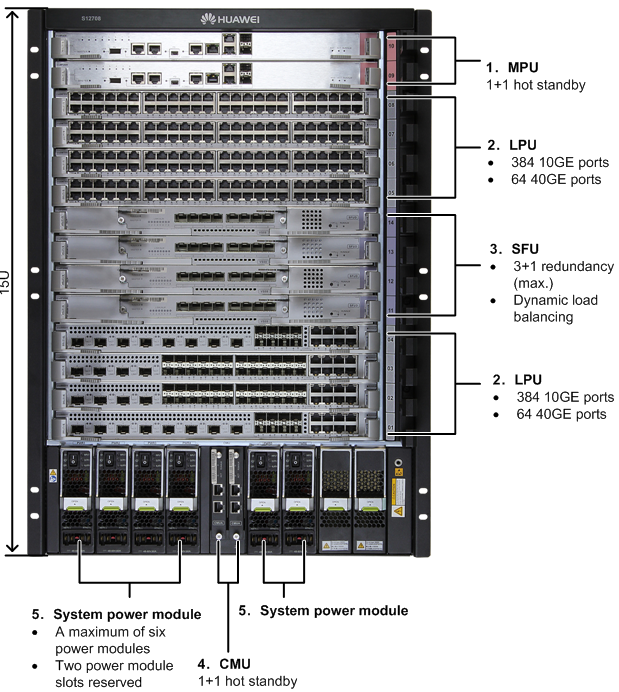
S12700 series agile switches



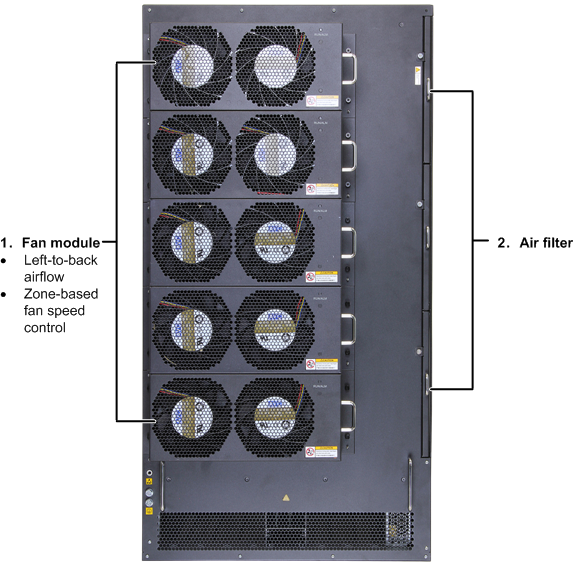
S12712 S12708

## S12708 Hardware architecture

S12708 front view

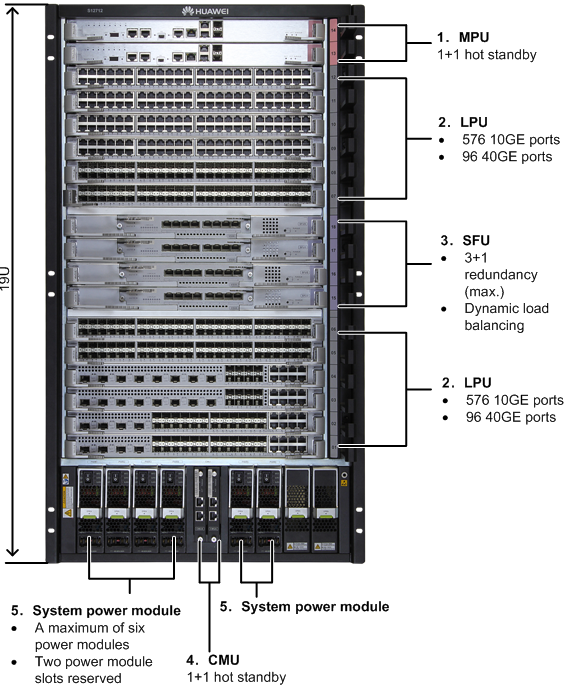


S12708 rear view

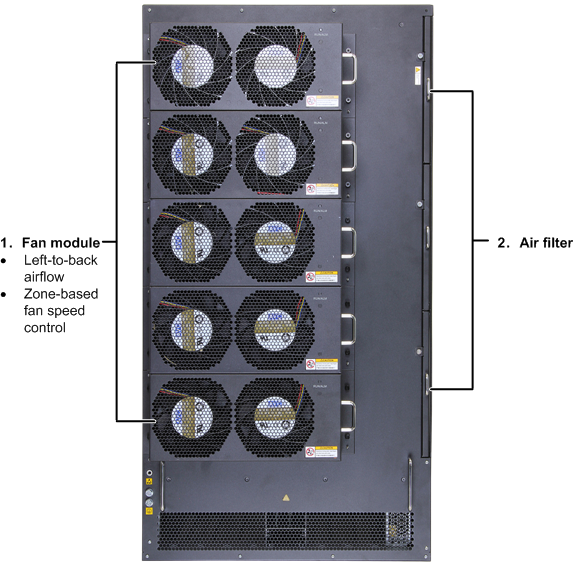


## S12712 Hardware architecture

S12712 front view



S12712 rear view

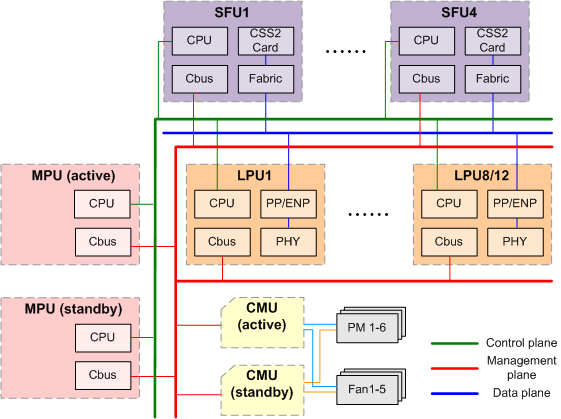


# Key Technologies

## S12700 System Architecture

The S12700 hardware separates control engines from switching engines. The MPUS and SFUs are independent of each other. Figure 2-1 shows the S12700 hardware architecture. The two MPUs provide the control plane and management plane, and the four SFUs complete data switching on the data plane. In addition, the S12700 has two CMUs to monitor and manage fans and power modules.

S12700 system architecture



This system architecture has the following characteristics:

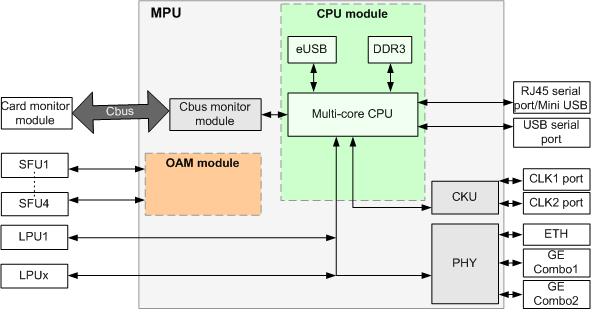
* The data plane, control plane, and management plane are independent from one another. The data plane completes service data switching; the control plane processes protocol packets; the management plane monitors and manages components using CAN Bus connections.
* Key hardware components support redundancy: 1+1 hot standby of MPUs, 3+1 hot standby of SFUs (load balancing among SFUs), 1+1 hot standby of CMUs, and M+N backup of power modules. A maximum of six power modules can be installed in a chassis, working in 1+1, 2+1, 2+2, 3+2, or 3+3 backup mode.
* The MPUs and SFUs are separated, so an MPU failure does not affect the switching performance. This architecture significantly improves device reliability.

## MPU Hardware Design

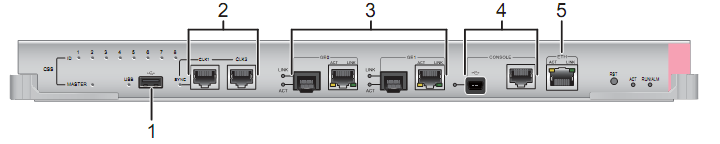
The S12700's MPU is ET1D2MPUA000, which provides the control plane and management plane for the entire system. The control plane provides functions such as protocol processing, service processing, route calculation, forwarding control, service scheduling, traffic statistics collection, and system security. The management plane is responsible for system status monitoring, environment monitoring, log and alarm processing, system software loading, and system upgrading. The ET1D2MPUA000 inherits powerful hardware OAM functions of the Sx7 series switches. It uses high-end field programmable gate array (FPGA) chips and high-speed storage chips to provide industry-leading hardware OAM detection performance.

| Model | Appearance |
| --- | --- |
| ET1D2MPUA000 |  |

MPU hardware architecture



S12700 MPU panel



| No. | Description |
| --- | --- |
| 1 | One USB port, used to load software from a UBS flash drive. |
| 2 | Two BITS ports (reserved). |
| 3 | Two GE ports (reserved). |
| 4 | One combo console port, consisting of a console port and a Mini USB port. The S12700 can connect to a console through this port for onsite configuration. |
| 5 | One ETH management port (10M/100M BASE-TX auto-sensing). It can connect to a network port of a configuration terminal or network management workstation to set up a local or remote configuration environment. |

The following table describes hardware parameters of the ET1D2MPUA000.

|  |  |
| --- | --- |
| Memory | 4 GB |
| eUSB | 2 GB, built-in. (The storage size is expandable, but the upgrade must be performed by Huawei. Customers cannot expand the storage size by themselves.) |
| External ports | * One 10/100M Ethernet port for software loading and out-of-band management * Two combo ports (GE0 and GE1) for clustering * One RS232 serial port used as a console port * One USB port for USB-based deployment |

## SFU Hardware Design

SFUs in a switch provides a data switching plane for the system. The data switching plane provides high-speed data channels to transmit data between LPUs. SFUs for the S12700 include ET1D2SFUA000, ET1D2SFUC000, and ET1D2SFUD000. The ET1D2SFUA000 and ET1D2SFUD000 apply to both the S12708 and S12712, whereas the ET1D2SFUC000 applies only to the S12708.

|  |  |
| --- | --- |
| Model | Appearance |
| ET1D2SFUA000 |  |
| ET1D2SFUC000 |  |
| ET1D2SFUD000 |  |

SFU hardware architecture



## Hardware Design of X1E Series Interface Cards

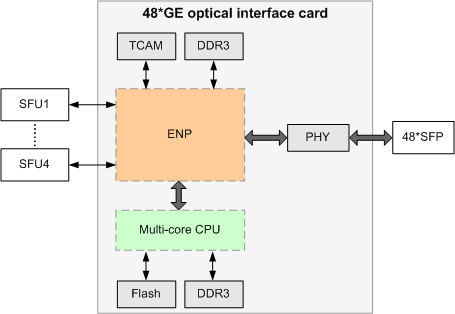
The S12700 series supports various LPUs with ENP chips, including ET1D2G48TX1E, ET1D2G48SX1E, ET1D2S04SX1E, and ET1D2S08SX1E. The X1E series LPUs provide programmability and support several million hardware entries, much more than those supported by traditional switches. Additionally, the X1E series LPUs have a large buffer capacity to prevent packet loss caused by traffic bursts.

|  |  |
| --- | --- |
| Model | Appearance |
| ET1D2G48TX1E | (48-port 10/100/1000BASE-T interface card) |
| ET1D2G48SX1E | (48-port 100/1000BASE-X interface card) |
| ET1D2S04SX1E | (4-port 10GBASE-X and 24-port 100/1000BASE-X and 8-port 10/100/1000BASE-T combo interface card) |
| ET1D2S08SX1E | (8-port 10GBASE-X and 8-port 100/1000BASE-X and 8-port 10/100/1000BASE-T combo interface card) |

The following figures show the hardware architecture of X1E series LPUs.

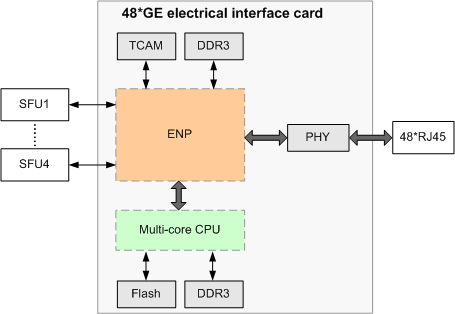
A 48\*GE interface card provides forty-eight 100/1000M Ethernet optical ports and uses the ENP chip. Figure 2-5 shows its hardware architecture.

Hardware architecture of a 48\*GE optical interface card



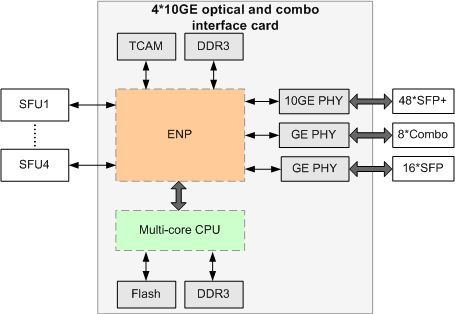
A 48\*GE optical interface card provides forty-eight 10/100/1000M auto-sensing Ethernet electrical ports. Figure 2-6 shows its hardware architecture.

Hardware architecture of a 48\*GE electrical interface card



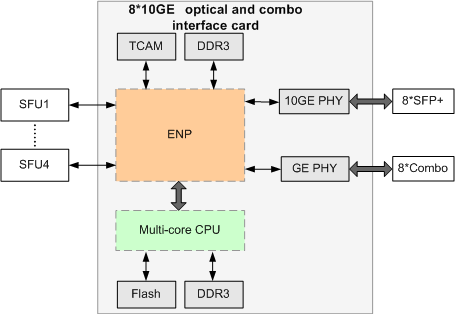
A 4\*10GE combo interface card provides four 10GE optical ports, twenty-four 100/1000M optical ports, and eight 10/100/1000M electrical ports. Eight of 100/1000M optical ports are multiplexed with the eight electrical ports. Figure 2-7 shows its hardware architecture.

Hardware architecture of a 4\*10GE optical and combo interface card



An 8\*10GE combo interface card provides eight 10GE optical ports, eight 100/1000M optical ports, and eight 10/100/1000M electrical ports. The eight 100/1000M optical ports are multiplexed with the eight electrical ports. Figure 2-8 shows its hardware architecture.

Hardware architecture of an 8\*10GE optical and combo interface card



## Hardware Design of a 48\*10GE Interface Card

The S12700 series supports 48\*10GE high-density line-speed interface cards and provide up to 576 10GE ports on a chassis. This high port density meets requirements of bandwidth-consuming scenarios such as multimedia video conferencing and data center communication. Figure 2-9 shows the hardware structure of a 48\*10GE optical interface card.

|  |  |
| --- | --- |
| Model | Appearance |
| ET1D2X48SEC0 |  |

Hardware architecture of a 48\*10GE optical interface card

